

10-Bit CMOS Voltage Output DAC in an8-Terminal Package 5-V Single Supply Operation **3-Wire Serial Interface High-Impedance Reference Inputs** Voltage Output Range ... 2 Times the Reference Input Voltage **Internal Power-On Reset** Low Power Consumption . . . 1.75 mW Max Update Rate of 1.21 MHz Settling Time to 0.5 LSB . . . 12.5 µs Typ **Monotonic Over Temperature** Pin Compatible With the Maxim MAX515applications **Battery-Powered Test Instruments Digital Offset and Gain Adjustment Battery Operated/Remote IndustrialControls Machine and Motion Control Devices Cellular Telephones**



description

The MC5615 is a 10-bit voltage output digital-to-analog converter (DAC) with a buffered reference input (high impedance). The DAC has an output voltage range that is two times the reference voltage, and the DAC is monotonic. The device is simple to use, running from a single supply of 5 V. A power-on-reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the MC5615 is over a three-wire serial bus that is CMOS compatible and easily interfaced to industry standard microprocessor and microcontroller devices. The device receives a 16-bit data word to produce the analog output. The digital inputs feature Schmitt triggers for high noise immunity. Digital communication protocols include the SPIE, QSPIE, and MicrowireE standards.

The 8-terminal small-outline D package allows digital control of analog functions in space-critical applications. The MC5615C is characterized for operation from 0°C to 70°C. The MC5615I is characterized for operation from –40°C to 85°C.

PACKAGE									
Τ _Α	SMALL OUTLINE [†] (D)	PLASTIC SMALL OUTLINE (DGK)	PLASTIC DIP (P)						
0°C to 70°C	MC5615 CD	TLC5615CDGK	MC5615CP						
-40°C to 85°C	MC561515ID	TLC5615IDGK	MC5615 IP						

AVAILABLE OPTIONS

† Available in tape and reel as the MC5615CDR and the MC5615IDR





Terminal Functions

TERMIN	IAL	1/0	DESCRIPTION	
NAME	NO.		DESCRIPTION	
DIN	1	1	Serial data input	
SCLK	2	- 1	Serial clock input	
CS	3	1	hip select, active low	
DOUT	4	0	Serial data output for daisy chaining	
AGND	5		Analog ground	
REFIN	6	I	Reference input	
OUT	7	0	DAC analog voltage output	
V _{DD}	8		Positive power supply	

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (VDD to AGND)	7V
Digital input voltage range to AGND	– 0.3 V to VDD + 0.3 V
Reference input voltage range to AGND	$\ldots \ldots - 0.3$ V to VDD + 0.3 V
Output voltage at OUT from external source	VDD + 0.3 V
Continuous current at any terminal	$\dots\dots\dots\pm 20\ \text{mA}$
Operating free-air temperature range, TA: MC5615C	0°C to 70°C
MC5615I	
Storage temperature range, Tstg	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	
† Stresses beyond those listed under "absolute maximum ratings" may cause permanent dam ratings only, and	age to the device. These are stress
functional operation of the device at these or any other conditions beyond those indicated und conditions" is not	er "recommended operating

implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, VDD	Supply voltage, V _{DD}		5	5.5	V
High-level digital input voltage, ∨ _{IH}		2.4			V
Low-level digital input voltage, VIL				0.8	V
Reference voltage, V _{ref} to REFIN terminal		2	2.048	$V_{DD}-2$	V
Load resistance, RL		2			kΩ
Operating free air temperature T	MC5615C	0		70	°C
Operating free-air temperature, 1A	MC5615I	-40		85	°C

electrical characteristics over recommended operating free-air temperature range, VDD = 5 V \pm 5%,

Vref = 2.048 V (unless otherwise noted)

static DAC specifications

	PARAMETER		TEST CON	DITIONS	MIN	TYP	MAX	UNIT
	Resolution				10			bits
	Integral nonlinearity, end point adjuste	ed (INL)	∨ _{ref} = 2.048 ∨,	See Note 1			±1	LSB
	Differential nonlinearity (DNL)		∨ _{ref} = 2.048 ∨,	See Note 2		±0.1	±0.5	LSB
EZS	Zero-scale error (offset error at zero scale)		∨ _{ref} = 2.048 ∨,	See Note 3			±3	LSB
	Zero-scale-error temperature coefficient		∨ _{ref} = 2.048 ∨,	See Note 4		3		ppm/°C
EG	Gain error		∨ _{ref} = 2.048 ∨,	See Note 5			±3	LSB
	Gain-error temperature coefficient		V _{ref} = 2.048 ∨,	See Note 6		1		ppm/°C
DODD	Power augustu releation ratio	Zero scale	See Notes 7 and	0	80			dB
PSRR	Power-supply rejection ratio	Gain	See Notes 7 and	°	80			ав
	Analog full scale output		RL = 100 kΩ		2\	/ref(1023/1024)		V

NOTES: 1. The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors (see text).

2. The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains

constant) as a change in the digital input code.

3. Zero-scale error is the deviation from zero-voltage output when the digital input code is zero (see text).

4. Zero-scale-error temperature coefficient is given by: EZS TC = [EZS (Tmax) – EZS (Tmin)]/Vref · 106/(Tmax – Tmin).

5. Gain error is the deviation from the ideal output (Vref – 1 LSB) with an output load of 10 k Ω excluding the effects of the zero-scale error.

6. Gain temperature coefficient is given by: EG TC = [EG(Tmax) – EG (Tmin)]/Vref · 106/(Tmax – Tmin).

7. Zero-scale-error rejection ratio (EZS-RR) is measured by varying the VDD from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.

8. Gain-error rejection ratio (EG-RR) is measured by varying the VDD from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero-scale change.

voltage output (OUT)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vo	Voltage output range	R _L = 10 kΩ	0	V	0D-0.4	V
	Output load regulation accuracy	$V_{O(OUT)} = 2 V$, $R_L = 2 k\Omega$			0.5	LSB
losc	Output short circuit current	OUT to V _{DD} or AGND		20		mA
VOL(low)	Output voltage, low-level	IO(OUT) ≤ 5 mA			0.25	V
VOH(high)	Output voltage, high-level	I _{O(OUT)} ≤ -5 mA	4.75			V





electrical characteristics over recommended operating free-air temperature range, $VDD = 5 V \pm 5\%$,

Vref = 2.048 V (unless otherwise noted) (continued)

reference input (REFIN)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VI	Input voltage		0		$V_{DD}-2$	V
ŋ	Input resistance		10			MΩ
Ci	Input capacitance			5		pF
				Ű.		

digital inputs (DIN, SCLK, CS)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIH	High-level digital input voltage		2.4			V
VIL	Low-level digital input voltage				0.8	V
Iн	High-level digital input current	VI = VDD			±1	μA
ηL	Low-level digital input current	∨ _I = 0			±1	μA
Ci	Input capacitance			8		pF

digital output (DOUT)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOH	Output voltage, high-level	I _O = -2 mA	V _{DD} -1			V
VOL	Output voltage, low-level	I _O = 2 mA			0.4	V

power supply

	PARAMETER	TEST COND	TIONS	MIN	TYP	MAX	UNIT
VDD	Supply voltage			4.5	5	5.5	V
ססי	Downer ownelly gurrent	V_{DD} = 5.5 V, No load, All inputs = 0 V or V_{DD}	∨ _{ref} = 0		150	250	μA
	Power supply current	V _{DD} = 5.5 V. No load, All inputs = 0 V or V _{DD}	∨ _{ref} = 2.048 ∨		230	350	μΑ
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analog output dynamic performance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise + distortion, S/(N+D)	V _{ref} = 1 V _{pp} at 1 kHz + 2.048 Vdc, code = 11 1111 1111, See Note 9	60			dB

NOTE 9: The limiting frequency value at 1 Vpp is determined by the output-amplifier slew rate.



digital input timing requirements (see Figure 1)

	PARAMETER	MIN	NOM	MAX	UNIT
t _{su(DS)}	Setup time, DIN before SCLK high	45			ns
^t h(DH)	Hold time, DIN valid after SCLK high	0			ns
t _{su(CSS)}	Setup time, CS low to SCLK high	1			ns
t _{su(CS1)}	Setup time, CS high to SCLK high	50			ns
th(CSH0)	Hold time, SCLK low to CS low	1			ns
th(CSH1)	Hold time, SCLK low to CS high	0			ns
tw(CS)	Pulse duration, minimum chip select pulse width high	20			ns
tw(CL)	Pulse duration, SCLK low	25			ns
tw(CH)	Pulse duration, SCLK high	25			ns

output switching characteristic

PARAMETER		TEST CONDITIONS		NOM	MAX	UNIT
tpd(DOUT)	Propagation delay time, DOUT	CL = 50 pF			50	ns

operating characteristics over recommended operating free-air temperature range, V_{DD} = 5 V ± 5%, V_{ref} = 2.048 V (unless otherwise noted)

analog output dynamic performance

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
SR	Output slew rate	C _L = 100 pF, R _L = 10 kΩ, T _A = 25°C	0.3	0.5		V/µs
ts Output settling time RL		To 0.5 LSB, CL = 100 pF, RL = 10 kΩ, See Note 10	.5 LSB, C _L = 100 pF, = 10 kΩ, See Note 10 12.5			μs
	Glitch energy	DIN = All 0s to all 1s		5		nV∙s

NOTE 10: Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 000 hex to 3FF hex or 3FF hex to 000 hex.

reference input (REFIN)

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PARAMETER	TEST CONDITIONS			TYP	MAX	UNIT
Reference feedthrough	REFIN = 1 Vpp at 1 kHz + 2.048 Vdc (see Note 11)		-80		dB	
Reference input bandwidth (f-3dB) REFIN = 0.2 Vpp + 2.0		REFIN = 0.2 ∨ _{pp} + 2.048 ∨dc		30		kHz

NOTE 11: Reference feedthrough is measured at the DAC output with an input code = 000 hex and a Vref input = 2.048 Vdc + 1 Vpp at 1 kHz.



PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input clock, applied at the SCLK terminal, should be inhibited low when CS is high to minimize clock feedthrough. B. Data input from preceeding conversion cycle.

C. Sixteenth SCLK falling edge









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general function

The MC5615 uses a resistor string network buffered with an op amp in a fixed gain of 2 to convert 10-bit digital data to analog voltage levels (see functional block diagram and Figure 9). The output of the MC5615 is the same polarity as the reference input (see Table 1).

An internal circuit resets the DAC register to all zeros on power up.



Figure 9. MC5615 Typical Operating Circuit

Table 1. Binary Code Table (0 V to 2 V_{REFIN} Output), Gain = 2

	INPUT [†]		OUTPUT
1111	1111	11(00)	2(V _{REFIN}) <u>1023</u> 1024
	:		:
1000	0000	01(00)	2(V _{REFIN}) <u>513</u> 1024
1000	0000	00(00)	$2(\vee_{REFIN})\frac{512}{1024} = \vee_{REFIN}$
0111	1111	11(00)	2(V _{REFIN}) <u>511</u> 1024
	:		:
0000	0000	01(00)	$2(\vee_{REFIN})\frac{1}{1024}$
0000	0000	00(00)	0 V

⁺ A 10-bit data word with two bits below the LSB bit (sub-LSB) with 0 values must be written since the DAC input latch is 12 bits wide.





buffer amplifier

The output buffer has a rail-to-rail output with short circuit protection and can drive a 2-k Ω load with a 100-pF load capacitance. Settling time is 12.5 μ s typical to within 0.5 LSB of final value.

external reference

The reference voltage input is buffered, which makes the DAC input resistance not code dependent. Therefore, the REFIN input resistance is 10 M Ω and the REFIN input capacitance is typically 5 pF independent of input code. The reference voltage determines the DAC full-scale output.

logic interface

The logic inputs function with either TTL or CMOS logic levels. However, using rail-to-rail CMOS logic achieves the lowest power dissipation. The power requirement increases by approximately 2 times when using TTL logic levels.

serial clock and update rate

Figure 1 shows the MC5615 timing. The maximum serial clock rate is:

f(SCLK)max _

1

tw_CH__tw_CL_

or approximately 14 MHz. The digital update rate is limited by the chip-select period, which is:

tp(CS)_16 __tw_CH_tw_CL___tw_CS_

and is equal to 820 ns which is a 1.21 MHz update rate. However, the DAC settling time to 10 bits of 12.5 $\mbox{$\mu$s}$

limits the update rate to 80 kHz for full-scale input step transitions.





serial interface

When chip select (CS) is low, the input data is read into a 16-bit shift register with the input data clocked in most significant bit first. The rising edge of the SLCK input shifts the data into the input register.

The rising edge of CS then transfers the data to the DAC register. When CS is high, input data cannot be clocked into the input register. All CS transitions should occur when the SCLK input is low.

If the daisy chain (cascading) function (see daisy-chaining devices section) is not used, a 12-bit input data sequence with the MSB first can be used as shown in Figure 10:



Figure 11. 16-Bit Input Data Sequence

The data from DOUT requires 16 falling edges of the input clock and, therefore, requires an extra clock width. When daisy chaining multiple MC5615 devices, the data requires 4 upper dummy bits because the data transfer requires 16 input-clock cycles plus one additional input-clock falling edge to clock out the data at the DOUT terminal (see Figure 1).

The two extra (sub-LSB) bits are always required to provide hardware and software compatibility with 12-bit data converter transfers.

The MC5615 three-wire interface is compatible with the SPI, QSPI†, and Microwire serial standards. The hardware connections are shown in Figure 12 and Figure 13.

The SPI and Microwire interfaces transfer data in 8-bit bytes, therefore, two write cycles are required to input data to the DAC. The QSPI interface, which has a variable input data length from 8 to 16 bits, can load the DAC input register in one write cycle.





serial interface (continued)



NOTE A: The DOUT-SI connection is not required for writing to the MC5615 but may be used for verifying data transfer if desired.



NOTE A: The DOUT-MISO connection is not required for writing to the MC5615 but may be used for verifying data transfer.

Figure 13. SPI/QSPI Connection

Figure 12. Microwire Connection daisy-chaining devices

DACs can be daisy-chained by connecting the DOUT terminal of one device to the DIN of the next device in the chain, providing that the setup time, tsu(CSS), (CS low to SCLK high) is greater than the sum of the setup time, tsu(DS), plus the propagation delay time, tpd(DOUT), for proper timing (see digital input timing requirements section). The data at DIN appears at DOUT, delayed by 16 clock cycles plus one clock width. DOUT is a totem-poled output for low power. DOUT changes on the SCLK falling edge when CS is low. When CS is high, DOUT remains at the value of the last data bit and does not go into a high-impedance state.

linearity, offset, and gain error using single ended supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V. The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 14.





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linearity, offset, and gain error using single ended supplies (continued)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage. For the MC5615, the zero-scale (offset) error is plus or minus 3 LSB maximum. The code is calculated from the maximum specification for the negative offset.

power-supply bypassing and ground management

Printed-circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane making sure that analog ground currents are well managed and there are negligible voltage drops across the ground plane.

A $0.1-\mu$ F ceramic-capacitor bypass should be connected between VDDand AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog supply from the digital power supply.

Figure 15 shows the ground plane layout and bypassing technique



Figure 15. Power-Supply Bypassing

saving power

Setting the DAC register to all 0s minimizes power consumption by the reference resistor array and the output load when the system is not using the DAC.

ac considerations

digital feedthrough

Even with CS high, high-speed serial data at any of the digital input or output terminals may couple through the DAC package internal stray capacitance and appear at the DAC analog output as digital feedthrough. Digital feedthrough is tested by holding CS high and transmitting 0101010101 from DIN to DOUT.

analog feedthrough

Higher frequency analog input signals may couple to the output through internal stray capacitance. Analog feedthrough is tested by holding CS high, setting the DAC code to all 0s, sweeping the frequency applied to REFIN, and monitoring the DAC output.





0.050 (1,27) 0.020 (0,51) \oplus 0.010 (0,25) M 0.014 (0,35) 14 8 0.008 (0,20) NOM 0.244 (6,20) 0.228 (5,80) 0.157 (4,00) 0.150 (3,81) Gage Plane 0.010 (0,25) 1 7 0°-8 0.044 (1,12) 0.016 (0,40) Seating Plane 0.010 (0,25) 0.004 (0,10) 0.069 (1,75) MAX 0.004 (0,10) PINS ** 8 14 16 DIM 0.197 0.344 0.394 A MAX (5,00)(8,75)(10,00)0.189 0.337 0.386 A MIN (4, 80)(8, 55)(9,80)

MECHANICAL DATA D (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-012





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MECHANICAL DATA P (R-PDIP-T8) PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001



MECHANICAL DATA DGK (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion.

D. Falls within JEDEC MO-187