

UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER GENERAL DESCRIPTION

The MSM82C51A-2 is a USART (Universal Synchronous Asynchronous Receiver Transmitter) for serial data communication.

As a peripheral device of a microcomputer system, the MSM82C51A-2 receives parallel data from the CPU and transmits serial data after conversion. This device also receives serial data from the outside and transmits parallel data to the CPU after conversion.

The MSM82C51A-2 configures a fully static circuit using silicon gate CMOS technology.

Therefore, it operates on extremely low power at 100 mA (max) of standby current by suspending all operations.

FEATURES

- Wide power supply voltage range from 3 V to 6 V
- Wide temperature range from -40 ° C to 85 ° C
- Synchronous communication upto 64 Kbaud
- Asynchronous communication upto 38.4 Kbaud
- Transmitting/receiving operations under double buffered configuration.
- Error detection (parity, overrun and framing)
- 28-pin Plastic DIP (DIP28-P-600-2.54): (Product name: MSM82C51A-2RS)
- 28-pin Plastic QFJ (QFJ28-P-S450-1.27): (Product name: MSM82C51A-2JS)
- 32-pin Plastic SSOP(SSOP32-P-430-1.00-K): (Product name: MSM82C51A-2GS-K)





FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)





FUNCTION

Outline

The MSM82C51A-2's functional configuration is programed by software.

Operation between the MSM82C51A-2 and a CPU is executed by program control. Table 1

shows the operation between a CPU and the device.

Table 1 Operation between MSM82C51A and CPU

CS	C/D	RD	WR	
1	×	×	×	Data Bus 3-State
0	×	1	1	Data Bus 3-State
0	1	0	1	$\text{Status} \rightarrow \text{CPU}$
0	1	1	0	$Control \ Word \leftarrow CPU$
0	0	0	1	$\text{Data} \rightarrow \text{CPU}$
0	0	1	0	Data ← CPU

It is necessary to execute a function-setting sequence after resetting the MSM82C51A-2. Fig. 1 shows the function-setting sequence.

If the function was set, the device is ready to receive a command, thus enabling the transfer of data by setting a necessary command, reading a status and reading/writing data.



Fig. 1 Function-setting Sequence (Mode Instruction Sequence)

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Control Words

There are two types of control word.

- 1. Mode instruction (setting of function)
- 2. Command (setting of operation)

1) Mode Instruction

Mode instruction is used for setting the function of the MSM82C51A-2. Mode instruction will be in "wait for write" at either internal reset or external reset. That is, the writing of a control word after resetting will be recognized as a "mode instruction." Items set by mode instruction are as follows:

- Synchronous/asynchronous mode
- Stop bit length (asynchronous mode)
- Character length
- Parity bit
- Baud rate factor (asynchronous mode)
- Internal/external synchronization (synchronous mode)
- Number of synchronous characters (Synchronous mode)

The bit configuration of mode instruction is shown in Figures 2 and 3. In the case of

synchronous mode, it is necessary to write one-or two byte sync characters.

If sync characters were written, a function will be set because the writing of sync characters constitutes part of mode instruction.



Fig. 2 Bit Configuration of Mode Instruction (Asynchronous)

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Fig. 3 Bit Configuration of Mode Instruction (Synchronous)



2) Command

Command is used for setting the operation of the MSM82C51A-2.

It is possible to write a command whenever necessary after writing a mode instruction and sync characters.

Items to be set by command are as follows:

- Transmit Enable/Disable
- Receive Enable/Disable
- $\overline{\text{DTR}}$, $\overline{\text{RTS}}$ Output of data.
- Resetting of error flag.
- Sending to break characters
- Internal
- Hunt mode (synchronous mode)

The bit configuration of a command is shown in Fig. 4.



Note: Seach mode for synchronous

charactors in synchronous mode.

Fig. 4 Bit Configuration of Command

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Status Word

It is possible to see the internal status of MSM82C51A-2 by reading a status word. The bit configuration of status word is shown in Fig. 5.



Fig. 5 Bit Configuration of Status Word

Standby Status

It is possible to put the MSM82C51A-2 in "standby status"

When the following conditions have been satisfied the MSM82C51A-2 is in "standby status."

(1) \overline{CS} terminal is fixed at Vcc level.

(2) Input pins other \overline{CS} , D0 to D7, \overline{RD} , \overline{WR} and C/\overline{D} are fixed at Vcc or GND level (including

SYNDET in external synchronous mode).

Note: When all output currents are 0, ICCS specification is applied.



Pin Description

Do to D7 (l/O terminal)

This is bidirectional data bus which receive control words and transmits data from the CPU and

sends status words and received data to CPU.

RESET (Input terminal)

A "High" on this input forces the MSM82C51A-2 into "reset status."

The device waits for the writing of "mode instruction."

The min. reset width is six clock inputs during the operating status of CLK.

CLK (Input terminal)

CLK signal is used to generate internal device timing.

CLK signal is independent of R X C or T X C.

However, the frequency of CLK must be greater than 30 times the R X C and T X C at Synchronous mode and Asynchronous "x1" mode, and must be greater than 5 times at Asynchronous "x16" and "x64" mode.

WR (Input terminal)

This is the "active low" input terminal which receives a signal for writing transmit data and control words from the CPU into the MSM82C51A-2.

R D (Input terminal)

This is the "active low" input terminal which receives a signal for reading receive data and status words from the MSM82C51A-2.

C/D (Input terminal)

This is an input terminal which receives a signal for selecting data or command words and status words when the MSM82C51A-2 is accessed by the CPU.

If $C/\overline{D} = low$, data will be accessed.

If C/D = high, command word or status word will be accessed.

C S (Input terminal)

This is the "active low" input terminal which selects the MSM82C51A-2 at low level when the CPU accesses.

Note: The device won't be in "standby status"; only setting C S = High.

Refer to "Explanation of Standby Status."

TXD (output terminal)

This is an output terminal for transmitting data from which serial-converted data is sent out.

The device is in "mark status" (high level) after resetting or during a status when transmit is

disabled. It is also possible to set the device in "break status" (low level) by a command.



TXRDY (output terminal)

This is an output terminal which indicates that the MSM82C51A-2 is ready to accept a

transmitted data character. But the terminal is always at low level if CTS = high or the device

was set in "TX disable status" by a command.

Note: TXRDY status word indicates that transmit data character is receivable, regardless of CTS or command. If the CPU writes a data character, TXRDY will be reset by the leading edge or \overline{WR} signal.

TXEMPTY (Output terminal)

This is an output terminal which indicates that the MSM82C51A-2 has transmitted all the characters and had no data character.

In "synchronous mode," the terminal is at high level, if transmit data characters are no longer

remaining and sync characters are automatically transmitted. If the CPU writes a data

character, TXEMPTY will be reset by the leading edge of WR signal.

Note : As the transmitter is disabled by setting CTS "High" or command, data written before disable will be sent out. Then TXD and TXEMPTY will be "High". Even if a data is written after disable, that data is not sent out and TXE will be "High".After the transmitter is enabled, it sent out. (Refer to Timing Chart of Transmitter Control and Flag Timing)

TXC (Input terminal)

This is a clock input signal which determines the transfer speed of transmitted data.

In "synchronous mode," the baud rate will be the same as the frequency of TXC.

In "asynchronous mode", it is possible to select the baud rate factor by mode instruction.

It can be 1, 1/16 or 1/64 the TXC.

The falling edge of TXC sifts the serial data out of the MSM82C51A-2.

RXD (input terminal)

This is a terminal which receives serial data.

RXRDY (Output terminal)

This is a terminal which indicates that the MSM82C51A-2 contains a character that is ready to READ.

If the CPU reads a data character, RXRDY will be reset by the leading edge of R D signal.

Unless the CPU reads a data character before the next one is received completely, the preceding data will be lost. In such a case, an overrun error flag status word will be set.

RXC (Input terminal)

This is a clock input signal which determines the transfer speed of received data.

In "synchronous mode," the baud rate is the same as the frequency of RXC.

In "asynchronous mode," it is possible to select the baud rate factor by mode instruction.

It can be 1, 1/16, 1/64 the R X C.



SYNDET/BD (Input or output terminal)

This is a terminal whose function changes according to mode.

In "internal synchronous mode." this terminal is at high level, if sync characters are received and synchronized. If a status word is read, the terminal will be reset. In "external synchronous mode, "this is an input terminal. A "High" on this input forces the MSM82C51A-2 to start receiving data characters. In "asynchronous mode," this is an output terminal which generates "high level"output upon the detection of a "break" character if receiver data contains a "low-level" space between the

stop bits of two continuous characters. The terminal will be reset, if RXD is at high level.

After Reset is active, the terminal will be output at low level.

D S R (Input terminal)

This is an input port for MODEM interface. The input status of the terminal can be recognized by the CPU reading status words.

D T R (Output terminal)

This is an output port for MODEM interface. It is possible to set the status of \overline{DTR} by a command.

C T S (Input terminal)

This is an input terminal for MODEM interface which is used for controlling a transmit circuit. The terminal controls data transmission if the device is set in "TX Enable" status by a command. Data is transmitable if the terminal is at low level.

RTS (Output terminal)

This is an output port for MODEM interface. It is possible to set the status $\overline{\text{RTS}}$ by a command.



ABSOLUTE MAXIMUM RATING

Parameter	Cumbol		Unit	Conditions		
Parameter	Symbol	MSM82C51A-2RS	MSM82C51A-2GS	MSM82C51A-2JS	Unit	Conditions
Power Supply Voltage	Vcc	-0.5 to +7			٧	With respect
Input Voltage	VIN	-0.5 to V _{CC} +0.5			٧	With respect to GND
Output Voltage	V _{OUT}	-0.5 to V _{CC} +0.5			٧	
Storage Temperature	T _{STG}	-55 to +150				—
Power Dissipation	PD	0.9 0.7 0.9			W	Ta = 25°C
				- II	1	

OPERATING RANGE

Parameter	Symbol	Range	Unit
Power Supply Voltage	Vcc	3 - 6	V
Operating Temperature	Top	-40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Тур.	Max.	Unit
Power Supply Voltage	Vcc	4.5	5	5.5	V
Operating Temperature	T _{op}	-40	+25	+85	°C
"L" Input Voltage	VIL	-0.3	—	+0.8	V
"H" Input Voltage	VIH	2.2	—	V _{CC} +0.3	V

DC CHARACTERISTICS

 $(V_{CC} = 4.5 \text{ to } 5.5 \text{ V} \text{ Ta} = -40^{\circ}\text{C to } +85^{\circ}\text{C})$

Parameter	Symbol	Min.	Тур.	Max.	Unit	Measurement Conditions
"L" Output Voltage	V _{OL}	_	—	0.45	V	I _{0L} = 2.5 mA
"H" Output Voltage	V _{OH}	3.7	_	_	V	I _{0H} = -2.5 mA
Input Leak Current	lu	-10		10	μA	$0 \le V_{IN} \le V_{CC}$
Output Leak Current	I _{L0}	-10	_	10	μA	$0 \le V_{OUT} \le V_{CC}$
Operating Supply Current	Icco	_	_	5	mA	Asynchronous X64 during Transmitting/ Receiving
Standby Supply Current	Iccs	_	_	100	μA	All Input voltage shall be fixed at V _{CC} or GND level.



AC CHARACTERISTICS CPU Bus Interface Part

 $(V_{CC} = 4.5 \text{ to } 5.5 \text{ V}, \text{ Ta} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Min.	Max.	Unit	Remarks
Address Stable before RD	t _{AR}	20		ns	Note 2
Address Hold Time for RD	t _{RA}	20	—	ns	Note 2
RD Pulse Width	t _{RR}	130	_	ns	_
Data Delay from RD	t _{RD}	-	100	ns	_
RD to Data Float	t _{DF}	10	75	ns	_
Recovery Time between RD	t _{RVR}	6	_	t _{CY}	Note 5
Address Stable before WR	t _{AW}	20	_	ns	Note 2
Address Hold Time for WR	t _{WA}	20	—	ns	Note 2
WR Pulse Width	t _{ww}	100	—	ns	_
Data Set-up Time for WR	t _{DW}	100	_	ns	—
Data Hold Time for WR	t _{WD}	0	_	ns	_
Recovery Time between WR	t _{RVW}	6	_	t _{CY}	Note 4
RESET Pulse Width	t _{RESW}	6	_	t _{CY}	_



Serial Interface Part

 $(VCC = 4.5 \text{ to } 5.5 \text{ V}, \text{ Ta} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter		Symbol	Min.	Max.	Unit	Remarks
Main Clock Period		t _{CY}	160	—	ns	Note 3
Clock Low Tme		tō	50	—	ns	_
Clock High Time		t _o	70	t _{CY} 50	ns	_
Clock Rise/Fall Time		t _{r,} t _f	_	20	ns	_
TXD Delay from Falling Edge of	TXC	t _{DTX}	_	1	μS	_
	$1 \times Baud$	f _{TX}	DC	64	kHz	
Transmitter Clock Frequency	$16 \times Baud$	f _{TX}	DC	615	kHz	Note 3
	$64 \times Baud$	f _{TX}	DC	615	kHz	
Transmitter Clock Low Time	$1 \times Baud$	t _{TPW}	13	—	t _{CY}	—
Transmiller Glock Low Time	16 \times , 64 \times Baud	t _{TPW}	2	—	t _{CY}	_
Transmitter Clock High Time	$1 \times Baud$	t _{TPD}	15	—	t _{CY}	-
mansmiller Glock might mile	16 \times , 64 \times Baud	t _{TPD}	3	—	t _{CY}	_
	$1 \times Baud$	f _{RX}	DC	64	kHz	
Receiver Clock Frequency	$16 \times Baud$	f _{RX}	DC	615	kHz	Note 3
	$64 \times Baud$	f _{RX}	DC	615	kHz	
Receiver Clock Low Time	$1 \times Baud$	t _{RPW}	13	—	t _{CY}	_
HECEIVEL CIUCK LOW TIME	16 \times , 64 \times Baud	t _{RPW}	2	_	t _{CY}	_
Receiver Clock High Time	$1 \times Baud$	t _{RPD}	15	—	t _{CY}	—
HECEIVEI CIOCK HIGH HIHE	16 \times , 64 \times Baud	t _{RPD}	3	—	t _{CY}	
Time from the Center of Last B TXRDY	t to the Rise of	t _{TXRDY}	—	8	t _{CY}	—
Time from the Leading Edge of of TXRDY	WR to the Fall	t _{txrdy} clear	_	400	ns	_
Time From the Center of Last B	it to the Rise of RXRDY	t _{RXRDY}	_	26	t _{CY}	_
Time from the Leading Edge of of RXRDY	RD to the Fall	t _{rxrdy} clear	_	400	ns	_
Internal SYNDET Delay Time fr	om Rising Edge of RXC	t _{IS}	_	26	t _{CY}	_
SYNDET Setup Time for RXC		t _{ES}	18	_	t _{CY}	_
TXE Delay Time from the Center of Last Bit		t _{txempty}	20	—	t _{CY}	_
MODEM Control Signal Delay Time from Rising Edge of WR		t _{wc}	8	_	t _{CY}	_
MODEM Control Signal Setup Time for Falling Edge of RD		t _{CR}	20	_	t _{CY}	_
RXD Setup Time for Rising Edg	e of RXC (1X Baud)	t _{RXDS}	11	_	t _{CY}	_
RXD Hold Time for Falling Edge	of RXC (1X Baud)	t _{RXDH}	17	_	t _{CY}	_

Notes: 1. AC characteristics are measured at 150 pF capacity load as an output load based on 0.8 V at low level and 2.2 V at high level for output and 1.5 V for input.

2. Addresses are CS and C/D.

3. fTX or fRX £ 1/(30 Tcy) 1' Baud

fTX or fRX £ 1/(5 Tcy) 16⁻, 64⁻ Baud

4. This recovery time is mode Initialization only. Recovery time between command writes for

Asynchronous Mode is 8 tCY and for Synchronous Mode is 18 tCY.

Write Data is allowed only when TXRDY = 1.

5. This recovery time is Status read only.

Read Data is allowed only when RXRDY = 1.

6. Status update can have a maximum delay of 28 clock periods from event affecting the status.

Version 1.0



TIMING CHART Sytem Clock Input



Transmitter Clock and Data



Receiver Clock and Data







Write Data Cycle (CPU ® USART)





Transmitter Control and Flag Timing (ASYNC Mode)



Note: The wave-form chart is based on the case of 7-bit data length + parity bit + 2 stop bit.

Receiver Control and Flag Timing (ASYNC Mode)



Note: The wave-form chart is based on the case of 7 data bit length + parity bit + 2 stop bit.



Transmitter Control and Flag Timing (SYNC Mode)

Note: The wave-form chart is based on the case of 5 data bit length + parity bit and 2 synchronous charactors.





Receiver Control and Flag Timing (SYNC Mode)

Note:

1. Internal Synchronization is based on the case of 5 data bit length + parity bit and 2 synchronous charactor.

2. External Synchronization is based on the case of 5 data bit length + parity bit.

Note: 1. Half-bit processing for the start bit

When the MSM82C51A-2 is used in the asynchronous mode, some problems are

caused in the processing for the start bit whose length is smaller than the 1-data bit

length. (See Fig. 1.)

Start bit Length	Mode	Operation
Smaller than 7-Receiver Clock Length	×16	The short start bit is ignored. (Normal)
Smaller than 31-Receiver Clock Length	×64	The short start bit is ignored. (Normal)
8-Receiver Clock Length	×16	Data cannot be received correctly due to a malfunction.
32-Receiver Clock Length	×64	Data cannot be received correctly due to a malfunction.
9 to 16-Receiver Clock Length	×16	The bit is regarded as a start bit. (normal)
33 to 64-Receiver Clock Length	×64	The bit is regarded as a start bit. (normal)

2. Parity flag after a break signal is received (See Fig. 2.)

When the MSM82C51A-2 is used in the asynchrous mode, a parity flag may be set when the next normal data is read after a break signal is received.

A parity flag is set when the rising edge of the break signal (end of the break signal) is changed between the final data bit and the parity bit, through a RXRDY signal may not be outputted.

If this occurs, the parity flag is left set when the next normal dats is received, and the received data seems to be a parity error.



Half-bit Processing Timing Chart for the Start bit (Fig. 1) Normal Operation

RXD	ST D ₀ D ₁ D ₂ D ₃ D ₄ D ₅ D ₆ D ₇ P SP	ST D ₀ D ₁ D ₂ D ₃ D ₄ D ₅ D ₆ D ₇ P SP					
RXRDY							
The Sta	The Start bit Is Shorter Than a 1/2 Data bit						
RXD		ST D ₀ D ₁ D ₂ D ₃ D ₄ D ₅ D ₆ D ₇ P SP					
RXRDY							
The Sta	art bit Is a 1/2 Data bit (A problem of MSM	82C51A-2)					
RXD		ST D ₀ D ₁ D ₂ D ₃ D ₄ D ₅ D ₆ D ₇ P SP					
RXRDY							
		A RXRDY signal is outputted during data reception due to a malfunction.					
The Sta	art bit Is Longer Than a 1/2 Data bit						
RXD		ST D ₀ D ₁ D ₂ D ₃ D ₄ D ₅ D ₆ D ₇ P SP					
RXRDY							
ST: SP: P: D₀ - D7	Start bit Stop bit Parity bit : Data bits						







NOTICE ON REPLACING LOW-SPEED DEVICES WITH HIGH-SPEED DEVICES

The conventional low speed devices are replaced by high-speed devices as shown below. When you want to replace your low speed devices with high-speed devices, read the replacement notice given on the next pages.

High-speed device (New)	Low-speed device (Old)	Remarks
M80C85AH	M80C85A/M80C85A-2	8bit MPU
M80C86A-10	M80C86A/M80C86A-2	16bit MPU
M80C88A-10	M80C88A/M80C88A-2	8bit MPU
M82C84A-2	M82C84A/M82C84A-5	Clock generator
M81C55-5	M81C55	RAM.I/O, timer
M82C37B-5	M82C37A/M82C37A-5	DMA controller
M82C51A-2	M82C51A	USART
M82C53-2	M82C53-5	Timer
M82C55A-2	M82C55A-5	PPI



Differences between MSM82C51A and MSM82C51A-2

1) Manufacturing Process

These devices use a 3 m Si-Gate CMOS process technology and have the same chip size.

2) Function

These devices have the same logics except for changes in AC characteristics listed in (3-2).

3) Electrical Characteristics

3-1) DC Characteristics

Parameter	Symbol	MSM82C51A	MSM82C51A-2
Vol measurement conditions	lol	+2.0 mA	+2.5 mA
VOH measurement conditions	Іон	-400 μA	-2.5 mA

al de

Although the output voltage characteristics of these devices are identical, but the measurement

conditions of the MSM82C51A-2 are more restricted than the MSM82C51A.

3-2) AC Characteristics

		Albin.	
Parameter	Symbol	MSM82C51A	MSM82C51A-2
RD Pulse Width	trr	250 ns minimum	130 ns minimum
RD Rising to Data Difinition	trd	200 ns maximum	100 ns maximum
RD Rising to Data Float	trf	100 ns maximum	75 ns minimum
WR Pulse Width	tww	250 ns minimum	100 ns minimum
Data Setup Time for WR Rising	tow	150 ns minimum	100 ns minimum
Data Hold Time for WR Rising	two	20 ns minimum	0 ns minimum
Master Clock Period	tcy	250 ns minimum	160 ns minimum
Clock Low Time	tō	90 ns minimum	50 ns minimum
Clock High Time	tφ	120 ns minimum tcy-90 ns maximum	70 ns minimum tcy-50 ns maximum

As shown above, the MSM82C51A-2 satisfies the characteristics of the MSM82C51A.



PACKAGE DIMENSIONS



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which

are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the

product name, package name, pin number, package code and desired mounting conditions

(reflow method, temperature and times).





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(reflow method, temperature and times).

4) Notices on use

Note the following when replacing devices as the ASYNC pin is differently treated between the MSM82C84A and the MSM82C84A-5/MSM82C84A-2:

Case 1: When only a pullup resistor is externally connected to.

The MSM82C84A can be replaced by the MSM82C84A-2.

Case 2: When only pulldown resistor is externally connected to.

When the pulldown resistor is 8 kiloohms or less, the MSM82C84A can be replaced by the MSM82C84A-2.

When the pulldown resistor is greater than 8 kiloohms, use a pulldown resistor of 8 kiloohms or less.

Case 3: When an output of the other IC device is connected to the device.

The MSM82C84A can be replaced by the MSM82C84A-2 when the IoL pin of the device to drive the

ASYNC pin of the MSM82C84A-2 has an allowance of 100 mA or more.